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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/680,625	10/06/2000	Daniel J. Lincoln	55110.US	9588

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EXAMINER	
MERID, ARADOM B	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 02/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/680,625	LINCOLN, DANIEL J.	
	Examiner	Art Unit	
	Aradom B. Merid	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/06/2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☒ Claim(s) *6-10 and 15-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 5 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites the limitation "... **said phase sync detect pattern**...." line 21-22 of claim 5. There is insufficient antecedent basis for this limitation in the claim.

Claim 14 recites the limitation "... **which of said multiple test data sets**...." line 18-20 page 24. There is insufficient antecedent basis for this limitation in the claim.

Claims 6-10 are inherently rejected because they are dependent of the rejected base claim 5.

Claims and 15-18 are also inherently rejected because they are dependent of the rejected base claim 14.

2. ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1 and 2 , are rejected under 35 U.S.C 102(e) as being anticipated by Malerevich et al. (U.S. Patent Number: 6,611,538 of record).

Regarding claims 1 and 2, Malerevich teaches an apparatus or a method for providing synchronization in data transmission system in which the system produces clock signals at the transmitting device and transmitting the clock signals(CLK1 and CLK2) to the receiving device(col. 5, lines 64-66 , col. 6,

lines 46-51 and Fig. 6 and 7). The transmission device also transmits a predetermined synchronization bits, which comprises two bits pattern(col. 2, lines 41-43 and), inserted in the data blocks (cells) at an interval of every cell cycle (col. 2, lines 9-12, and col.9, lines 16-18 of claim 1) from the transmitter to the receiver on parallel data lines (or multiple data lines) to insure synchronization of the parallel data transmission(col. 1, lines 26-31 and col.2, lines 50-62). On the receiving end the receiving device comprises a means for searching the two-bit synchronization sequence repeatedly to **align** the received parallel data with the boundaries of the cells by checking (extracting) the sequence pattern, which implies the receiver compensates any phase or bit delay of the received parallel data after extracting the synchronization sequence (col. 2, lines 3-11 and col. 9, lines 33-38 of claim 1).

Therefor, the above discussion may clearly be read to teach the claim limitations of claims 1 and 2.

3. ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malerevich et al. (U.S. Patent Number: 6,611,538 of record) in view of Hogeboom (U.S. Patent Number: 6,262,998 of record).

Malerevich discusses the transmission of data signals on multiple lines (4 data lines) which comprises multiple differential lines (4 differential lines) and the clock signal on one differential clock signal (col. 4, lines 1-3). Malerevich further discusses that the data (16 bit data) are sampled (or clocked) by the shift registers **50** every CLK1 cycle at the transmitter's input (Fig. 6) and the data are then transmitted to the receiver via the multiple differential lines every CLK1 cycle (col. 6, lines 1-11).

Malerevich does not disclose clocking (or sampling) the transmitted data in a bi-phase manner that is clocking the data at half of the data rate as mentioned in the specification of the applicant (page 9, line 4-5).

Hogeboom, however, discloses a data bus having both a synchronous clock and a channel of data, wherein the high and low period of the clock signal is one bit time of the data (see abstract) is used to recover the data (col. 4, lines27- 32), i.e. data is sampled during the high and low period of the clock. Hogeboom further discloses that the high and low periods (bi-phase) of the clock is an integer multiple of the one bit time of the data, which means that the data frequency is an integer multiple of the clock frequency(col.3, lines 19-25) and also as disclosed in the applicant specification(page 9, line 4-5).

In order to allow maximum data rate, and optimum matching between clock and data one of ordinary skill in the art would be motivated to incorporate Hogeboom's method (or apparatus) of clocking (sampling) the transmitted data in bi phase manner such that the even bits are transmitted during high period of the clock and the odd bits are transmitted during low clock period in Malerevich's claimed invention.

Therefore, applying Hogeboom's method (apparatus) in Malerevich's method (or apparatus) would have been obvious to one of ordinary skill in the art at the time the invention was made.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5 ,8, 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malerevich et al. (U.S. Patent Number: 6,611,538 of record) in view of Isozaki et al (U.S. Patent Number: 6,470,142 of record) and in view of Kosaka et al (U.S. Patent Number: 5,040,195 of record).

Malerevich teaches a transmitting device (Fig. 5 and Fig. 6) that comprises a synch pattern generator **48,** which provides a predetermined synch

pattern, a clock generator **68** that generates CLK1 and CLK2, a mulitplexer **42** (mux) for multiplexing different group of transmitted data streams and synch sequence (or pattern) on 16 bit data lines (as recited in claim 5,8 and 12), and a controller **44** to control the mux **42** to transmit the selected sync sequence on each 16 bit data lines to the receiving device as (as recited in claim 5 and 12) (col. 5, line35 – col. 6, line 27, and claim1 on col. 9).

Malerevich also teaches a receiving device (Fig. 7 and Fig.8) that comprises a clock receiving circuit **84** for sampling (clocking) the transmitted data at CLK2 clock rate (twice the CLK1 rate) at the sampling shift registers **80** composed of 16 registers as claimed in claim 10 (4 blocks of shift registers and each block having 4 registers) each with four bit serial shift registers for receiving and sampling the data streams from the transmitter and outputting 16 bit parallel lines data to determine the sync sequence or pattern (as recited in claim 5) (col. 6, lines 27-44).

Malerevich, however, fails to teach a receiving device with a comparator for comparing the synchronization pattern and storing the amount of phase or time shift in memory and a test line controller on one of the parallel signal data as a sync detect.

Isozaki, however, teaches a parallel data synchronization detecting device **132** (Fig. 29) wherein synchronization of two sync pattern blocks of data length L and K is performed repeatedly with the output of the sync comparing **14** circuit at the comparing devices or comparator (**12** and **13** of Fig. 29). The comparing (L)

circuit **12** supplies a detected result and shift amount as a signal CL to the sync detecting **15** circuit. Likewise, the comparing(**K**) circuit 13 supplies a detected result and shift amount as a signal CK to the sync detecting **15** circuit to reduce data skewing (as recited in claim 5). The sync information which is the output of the sync detecting circuit **15** is supplied to a phase controlling circuit **16** which controls the phase of the sync information and supplies (writes) the result to memory storage RAM **17** (as recited in claim 5). The output of the memory RAM **17** is supplied to the output controlling circuit **20** to produce a synchronized final data. Isozaki also teaches that the data synchronization detecting device **132** with shift registers of **L10** and **K11** having bit lengths corresponding to the data length L, and the data length K respectively . (Col.34, line 42- Col. 35, line 17).

And Kosaka teaches a synchronizing signal line, as a test line controller, to detect and contol the synchronization of the remaining parallel data lines in order to recover the synchronization quickly (as recited in claim limitation 5) (col. 1, line 66-col.2, line2 and col. 3, lines 1-7).

Therefore, implementing Isozaki's method (or apparatus) of comparing the synch pattern blocks of data length L and data length K and storing the detected result in time or phase shift in memory (RAM) in order to prevent jittering or data skewing in combination with Kasaka's method (or apparatus) in order to reduce the computational time, and to transmit data at higher rate in

Malerevich's invention would have been obvious to one of ordinary skill in the art at the time the invention was made.

5. ***Allowable Subject Matter***

Claim14 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

Claims 6,7, 9, 11, 13 and 15-18 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

The following references also discuss about data synchronization and were considered because of their relevance to the application.

Nakamura et al.	U.S. Patent Number: 6,385,213
Tanka et al.	U.S. Patent Number: 5,867,541
Ducaroir et al.	U.S. Patent Number: 6,061,747
Sinniger et al.	U.S. Patent Number: 4,538,262
Asano et al.	U.S. Patent Number: 5,793,988
Ducaroir et al.	U.S. Patent Number: 6,330,591
Thomas et al.	U.S. Patent Number: 4,924,463
Kolblin et al.	U.S. Patent Number: 6,516,364
Wagner et al.	U.S. Patent Number: 4,389,544

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aradom B. Merid whose telephone number is 703-305-8953. The examiner can normally be reached on 8:00am-5:00pm (Mon. - Fri.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 703-306-3034. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Aradom B. Merid